09-15-05

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Schmidt, *et al.*	Docket No.:	INTECH 3.0-037 02 P 01514
Serial No.:	10/671,123	Art Unit:	2823
Filed:	September 24, 2003	Examiner:	William M. Brewster
For:	Structure and Method for Placement, Sizing and Shaping of Dummy Structures		

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Date of Deposit: September 14, 2005

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Certificate of Mailing via Express Mail (1 page)
Fee Transmittal (1 original and 1 copy)
Appeal Brief with Appendices (in triplicate) (111 pages)
Two (2) Return Postcards

Respectfully submitted,

KHayes

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PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Effective on 12/8/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/671,123
Filing Date	September 24, 2003
First Named Inventor	Schmidt, *et al.*
Examiner Name	William M. Brewster
Art Unit	2823
Attorney Docket No.	INTECH 3.0-037 02 P 01514

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 50-1065 Deposit Account Name: Slater & Matsil, L.L.P.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	$0.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 20 or HP =	0	x	$50.00	=	$ 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 3 or HP =	0	x	$200.00	=	$ 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
$360.00	0.00

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
	- 100 =		/ 50 =		(round up to a whole number) x	$250.00	=	$ 0.00

4. OTHER FEE(S) Fees Paid($)

Non-English Specification, $130 fee (no small entity discount)

Other: Filing a Brief in Support of an Appeal (Fee Code 1402) $500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 46,836	Telephone 972-732-1001
Name (Print/Type)	Roger C. Knapp		Date September 14, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Sebastian Schmidt	Docket No.:	INTECH 3.0-037 02 P 01514
Filed:	September 24, 2003	Examiner:	William M. Brewster
Serial No.:	10/671,123	Art Unit:	2823
For:	Structure and Method for Placement, Sizing and Shaping of Dummy Structures		

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Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed April 15, 2005. A Notice of Appeal was filed by facsimile on July 15, 2005.

REAL PARTY IN INTEREST

The present application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1-4 stand finally rejected. No claims have been allowed. Claims 1-4 are the subject of this appeal. The claims on appeal are reproduced in the attached Appendix.

STATUS OF AMENDMENTS

No Amendments have been entered after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention of claims 1-4 relates to microelectronic devices and micro-mechanical and micro-electromechanical devices (either type or both types hereinafter, "MEMs"). Application, page 1, ¶ 1. In particular, it relates to providing dummy structures on a substrate during the fabrication to achieve more uniform etching rates and rates at which the height of features of a layer are reduced during planarization processes, such as chemical mechanical polishing (CMP). Application, page 1, ¶ 1.

Generally, microelectronic devices and MEMs are fabricated by depositing and patterning layers of material on a substrate. During this fabrication, it is important that some processes occur at a uniform rate. For example, photoresist materials are commonly used to pattern underlying materials. This process involves depositing a layer of photoresist material over a surface of a substrate. The photoresist material is exposed to a light source in accordance with a pattern, and then exposed to a developer solution to remove the unwanted photoresist material.

A problem occurs when the layer of the photoresist material contains features of differing sizes and densities. In particular, the differing sizes and densities cause a variation in the concentration of the reactants in the developer solution. As a result, the photoresist material in

densely patterned areas is removed at a slower rate than less densely populated areas. Chemical etching is another example of this problem. Application, pages 1-2, ¶ 3.

A similar result occurs during a CMP process wherein dense functional areas are planarized at a lower rate than other areas. In this case, a non-planar surface may result, which may adversely affect subsequent processing steps. Application, page 2, ¶¶ 5-6.

In an attempt to improve the uniformity of the etching/polishing rate, dummy structures are added to prevent variation in material layer thickness during fabrication of the chip. Application, pages 3-4, ¶ 9. Dummy structures are not electrically active elements, but serve to raise the pattern density in areas of the wafer. Application, pages 3-4, ¶ 9. If dummy structures are present, the density of structures will be more uniform, resulting in more uniform layer thickness during material removal or deposition. Application, page 3, ¶ 9.

Previous attempts have focused on arbitrarily placing dummy structures in areas of the chip surface to improve the density of structures. Application, page 4, ¶ 9. However, placing dummy structures arbitrarily on the surface of a chip has limitations with respect to improving the yield and reliability of the processes. Application, page 4, ¶ 12.

Appellant's invention as recited in claim 1 aims to overcome these limitations by determining the density and location of the functional areas and then adding dummy structures as a function of the determined density and location of the functional areas. An example is illustrated in Figure 2 of the Application, wherein reference numerals 105, 110, and 115 indicate functional areas, and reference numerals 155-1 to 155-2 and 160-1 to 160-5 indicate dummy structures. Application, pages 7-8, ¶ 23. The placement of the dummy structures is based upon the density and width of the functional areas 105, 110, and 115 as described, for example, in paragraphs 24-30 of the Application. When the placement, shape, and size of the dummy

structures are so designed as to conform to the pattern of neighboring functional areas, the resulting density of structures on the layer will be uniform. Application, page 12 ¶ 39. With uniform density, optimum process control is achieved. Application, page 12 ¶ 39. In this manner, the etching/polishing rate may be more uniform.

Furthermore, as recited in Appellant's dependent claim 2, Appellant's invention also determines the placement of dummy structures as a function of the width and density of functional areas within a predetermined distance of a location, and the size of the dummy structures as a function of the determined placement. Dependent claim 3 claims a method of claim 2 further comprising determining a shape of said one dummy structure as a function of the determined size.

Claim 4 claims a method for use in fabricating a chip, by determining a density and location of functional areas of a layer in relation to a location being processed; and adding dummy structures to said layer as a function of the determined density and determined location, said dummy structures each having placement determined as a function of the width and density of the functional areas, size determined as a function of the determined placement, and shape determined as a function of the determined size.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4 stand rejected under 35 U.S.C. 102(e) as being anticipated by Tomita, U.S. Publication No. 2003/0102562 A1 ("Tomita").

ARGUMENT

It is respectfully submitted that claims 1-4 recite patentable subject matter under the provisions of 35 U.S.C. § 102.

REJECTION UNDER 35 U.S.C. §102(E) OVER TOMITA, U.S. PUBLICATION NO. 2003/0102562 A1 ("TOMITA").

Claims 1 and 4:

The Examiner finally rejected claims 1 and 4 under 35 U.S.C. § 102 as being anticipated by Tomita, U.S. Publication No. 2003/0102562 A1 ("Tomita"). To save space, these rejections will not be repeated herein. Relevant aspects of the rejections will be discussed in the Appellant's arguments.

Argument 1:

Briefly, the reference cited by the Office Action, Tomita, does not teach or suggest adding dummy structures "as a function of the determined density and determined location" of the functional area as recited in Appellant's claim 1. Rather, Tomita merely teaches that dummy patterns are simply placed wherever there is vacant space, *regardless of the density and location of neighboring functional areas*. In fact, Tomita discloses that large and small dummy patterns may be placed in vacant spaces "*as long as the dummy patterns are regularly arranged* to facilitate a control of process." Tomita, ¶ 76. Tomita places the regularly arranged large and small dummy patterns in any available vacant space. For example, FIG. 1 of Tomita illustrates that the large dummy patterns 11b are used wherever the vacant space is large enough to accommodate the large dummy patterns 11b. Small dummy patterns 11a fill in vacant spaces in which the large dummy patterns will not fit. The only factor that Tomita considers in placing the dummy patterns is gaps around or between actual patterns. *See, e.g.*, Tomita, ¶ 71. Tomita does not teach or suggest that dummy patterns are to be placed according to the density of functional areas.

In contrast, claim 1 of the present application recites a method to add dummy structures according to the density and location of neighboring functional structures. Application, claim 1. As illustrated in Figure 2 of the Application, the dummy structures are not regularly spaced in all vacant areas as disclosed in Tomita, but rather are positioned as *a function of the density and location* of the functional areas.

The Office Action's assertion that Tomita anticipates the present application because placement of dummy patterns in Tomita "is in fact a function of the determined density and determined location" is incorrect. *See* Advisory Action, dated June 6, 2005. As discussed above, Tomita merely adds dummy patterns in all vacant spaces regardless of the density of the functional areas. Assuming, only for the sake of argument, that there is a (very) loose correlation between the location of the functional areas and the location of the vacant space, the same cannot be said for the *density* of the functional areas and the vacant space - there is simply no relationship between the vacant space and the density of the functional areas.

For example, for any given size and shape of vacant space, Tomita teaches regularly placing dummy patterns. Notably, the placement of the dummy patterns for a given size and shape of vacant space *is the same regardless of the* ***density*** *of neighboring functional areas*. How can it be asserted that Tomita discloses adding dummy patterns as a function of the density of the functional area if the pattern obtained for a given size and shape of vacant space remains the same for all possible densities of the neighboring functional areas? Clearly, Tomita does not disclose adding dummy structures as a function of the density and location as recited in Appellant's claim 1.

As another example, assume that a vacant space having a given size and shape is provided. In Tomita, the dummy structures may be added *without any further knowledge of the*

surrounding area. In Appellant's invention as recited in claim 1, this is not the case. Appellant's invention adds dummy structures as a function of the surrounding functional areas. How can Tomita be said to disclose "adding dummy structures to said layer as a function of the determined density and determined location" if the dummy structures of Tomita may be added with ***no*** knowledge of the surrounding functional area? This example clearly illustrates the differences between Tomita and Appellant's invention as recited in claim 1, and highlights the fact that Tomita does not disclose the steps of Appellant's claim 1.

Tomita must disclose each and every element as set forth in Appellants' claim 1 for Tomita to anticipate Appellant's claim 1. (See MPEP § 2131, 8th Ed., Rev. 2, May 2004.) In this case, the question is whether or not Tomita discloses the steps of "determining a *density and location* of at least one functional area of a layer" and "adding dummy structures to said layer as a function of *the determined density and determined location.*" As discussed above, Tomita fails to disclose either of these steps, particularly determining the density of the functional area and adding dummy structures as a function of the determined density. In fact, Tomita simply discloses regularly arranging dummy patterns in vacant spaces *without* consideration of the density of the functional areas. Accordingly, Appellant submits that Tomita does not anticipate Appellant's claim 1.

Claim 4 includes similar limitations and is patentable for at least some of the same reasons as discussed above with reference to claim 1.

Claims 2 and 4

The Examiner finally rejected claims 2 and 4 under 35 U.S.C. § 102 as being anticipated by Tomita, U.S. Publication No. 2003/0102562 A1("Tomita"). To save space, these rejections

will not be repeated herein. Relevant aspects of the rejections will be discussed in the Appellant's arguments. Arguments above for claim 1 are incorporated herein. Additional arguments are presented herein.

Argument 1:

Tomita does not disclose the step of "determining a placement of said one dummy structure as *a function of the width and density of functional areas* within a predetermined distance of a location" as recited in Appellant's claim 2. In fact, the geometry of individual dummy structures is irrelevant in Tomita, which merely considers the active pattern 9 as a whole to determine the placement of dummy structures. Tomita, ¶ 64. Nowhere in Tomita is there a discussion, mention or even a suggestion that the width and density of the functional area be a factor in determining the placement of the dummy structures.

The final Office Action cited Tomita, ¶¶ 73-76 as supporting this assertion. For reference, Tomita, ¶¶ 73-76 is provided below.

> [0073] Further, by arranging the large dummy patterns 11b and the small dummy patterns 11a, the small dummy patterns 11a are not partly clustered, whereby the uniformity of the abrading rate by the CMP method is improved, and it is possible to prevent the isolating oxide film 13a from remaining on the nitride film by underpolishing. The isolating oxide film 13a on the large dummy patterns 11b and the relatively wide actual pattern 9 as the opening at the center thereof by pre-etching performed before the abrading step by the CMP method, whereby the isolating oxide film 13a is easily abraded, and problems caused by underpolishing do not occur.
>
> [0074] Further, a dominating ratio of the dummy patterns 11 and the isolating oxide film 13a of the active regions 9 and 11 with respect to an entire area is in a range of about 50 through 80%, which is in a level similar to that in the region where the actual patterns 9 are clustered. Accordingly, uniformity of the abrading rate by the CMP method is further improved on an entire surface of the semiconductor substrate 12.
>
> [0075] As described, in Embodiment 1, because the uniformity of the abrading

> rate is improved when the isolating oxide film 13a is abraded by the CMP method when the elements are isolated, it is possible to obtain the semiconductor device with preferable surface flatness and high reliability.
>
> [0076] The dimensions of the small dummy patterns 11a are appropriately set within a range of 1 through 100 times of the minimum dimensions of the actual patterns 9. The dimensions of the large dummy patterns 11b are appropriately set within a range of 10 through 1,000 times of the minimum dimension of the actual patterns 9. The dummy patterns 11, i.e. the small dummy patterns 11a and the large dummy patterns 11b, may be shaped like not only a rectangular but also a strap, a hook, and lines and spaces as long as the dummy patterns are regularly arranged to facilitate a control of process.

Where in this section does Tomita disclose the step "determining a placement of said one dummy structure as a function of the width and density of functional areas within a predetermined distance of a location"? At most, this section discloses a range of *sizes*, not a *placement*, for the dummy structures in terms of a "minimum dimension." It should be noted that the minimum dimension is not the same as the width of the functional area. The functional area may be many times the minimum size possible for a functional area.

Furthermore, Appellant's claim 2 requires that the functional areas "within a predetermined distance of a location" be used to determine the placement of the dummy structure. The Office Action has not identified, and Appellant cannot find, any discussion in Tomita wherein the functional areas "within a predetermined distance of a location" are utilized to determine a placement of dummy structures.

Upon review of these paragraphs cited by the final Office Action, it is clear that these paragraphs fail to disclose the step of "determining a placement of said one dummy structure as a function of the width and density of functional areas within a predetermined distance of a location" as recited in Appellant's claim 2.

Claim 4 includes similar limitations and is patentable for at least some of the same reasons as discussed above with reference to claim 2.

Argument 2:

Tomita does not teach or suggest the step of "determining a size of said one dummy structure as a function of the determined placement" as recited in Appellant's claim 2. The sizes of the dummy patterns in Tomita are selected as being "relatively small" or "relatively large" based only on the gaps into which they will be placed. Tomita, ¶¶ 64-65. Tomita discloses an illustrative example of "large dummy patterns" as being "18μm square . . . [with] a pitch of 20μm" and "small dummy patterns" as being "3μm square . . . [with] a pitch of 5μm". Tomita ¶ 65. The absolute sizes of the dummy patterns in Tomita are arbitrarily set as being "within a range of 1 through 100 times of the minimum dimensions of the actual patterns." Tomita, ¶ 76. Furthermore, Tomita discloses that the dummy structures are to be uniformly sized, shaped, and placed for process control. Tomita, ¶ 76.

In contrast, Appellant's claim 2 recites that the size of the dummy structures are determined as a function of the determined placement, which is a function of the width and density of the functional areas within a predetermined distance of a location. Thus, neighboring dummy structures may have differing sizes and shapes depending on the size, shape, and location of their respective neighboring functional areas.

The final Office Action cites Tomita, ¶¶ 73-76, which paragraphs are duplicated above, as disclosing this step. As discussed above, these paragraphs simply disclose a range of sizes of the dummy structures in terms of a "minimum dimension." The minimum dimension is not the same

as the width of the functional area. Rather, the functional area may have a width many times the minimum size possible for a functional area.

Therefore, Tomita does not anticipate the present application in determining the size of the dummy structures as a function of the density of surrounding functional areas.

Claim 4 includes similar limitations and is patentable for at least some of the same reasons as discussed above with reference to claim 2.

Claims 3 and 4

The Examiner finally rejected claims 3 and 4 under 35 U.S.C. § 102 as being anticipated by Tomita, U.S. Publication No. 2003/0102562 A1 ("Tomita"). To save space, these rejections will not be repeated herein. Relevant aspects of the rejections will be discussed in the Appellant's arguments. Arguments above for claims 1 and 2 are incorporated herein. An additional argument is presented herein.

Argument 1:

Tomita does not disclose the step of "determining a shape of said one dummy structure as a function of the determined size" as recited in Appellant's claim 3. In fact, Tomita decides the shape of the dummy structure arbitrarily. *See* Tomita, ¶ 76. Although Tomita allows for shapes that are not rectangles, such allowance is not based on any functional relationship between the shape and the size of the dummy structure. Tomita, ¶ 76 ("the dummy patterns ... may be shaped like not only a rectangular [sic] but also a strap, a hook, and lines and spaces"). Tomita thus discloses that the shapes are selected arbitrarily.

In contrast, Appellant's claim 3 recites that the shape of each dummy structure is determined as a function of the size of the dummy structure. Moreover, the size is determined from the placement of the dummy structure, which in turn is determined from the density and location of neighboring functional features. Application, claims 1-2. Thus, the shape of the dummy structure is related to the density of functional areas.

Thus, because Tomita does not disclose that shapes of each dummy structure are related to the density of structures in the functional area of the chip, Tomita does not anticipate Appellant's claim 3 in determining the shape of each dummy structure as a function of the size of the dummy structure.

Claim 4 includes similar limitations and is patentable for at least some of the same reasons as discussed above with reference to claim 3.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of claims 1-4 under 35 U.S.C. § 102 is improper and respectfully requests that the Board of Patent Appeals and Interference so find and reverse the Examiner's rejections.

To the extent necessary, Appellant petitions for an Extension of Time under 37 C.F.R. § 1.136. Please charge any fees, or credit any overpayments, in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 50-1065.

Respectfully submitted,

September 14, 2005
Date

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CLAIMS APPENDIX

APPEALED CLAIMS

1. (Original) A method for use in fabricating a chip, the method comprising the steps of:

determining a density and location of at least one functional area of a layer; and

adding dummy structures to said layer as a function of the determined density and determined location.

2. (Original) The method of claim 1 wherein for at least one of the dummy structures, the adding step includes the steps of:

determining a placement of said one dummy structure as a function of the width and density of functional areas within a predetermined distance of a location; and

determining a size of said one dummy structure as a function of the determined placement.

3. (Original) The method of claim 2 further comprising determining a shape of said one dummy structure as a function of the determined size.

4. (Original) A method for use in fabricating a chip, the method comprising the steps of:

determining a density and location of functional areas of a layer in relation to a location being processed; and

adding dummy structures to said layer as a function of the determined density and determined location, said dummy structures each having placement determined as a function of the width and density of the functional areas, size determined as a function of the determined placement, and shape determined as a function of the determined size.

EVIDENCE APPENDIX

Included in this Appendix is:

A copy of U.S. Patent Application Publication No. US 2003/0102562 to Tomita *(relied upon by Examiner in Office Action dated April 15, 2004).*